**Amendment of the Claims**

Please cancel claims 13-16.

1. (Original) A magnetic random access memory (MRAM) device comprising:

an array of magnetic memory cells;

a plurality of word and bit lines connecting columns and rows of the memory cells so that the memory cells are positioned at cross-points of the word and bit lines, each memory cell having a magnetic reference layer and a magnetic data layer, each magnetic reference layer and each magnetic data layer having a magnetization that is switchable between two states under the influence of a magnetic field, each reference layer having at a first temperature a coercivity that is lower than that of each data layer at the first temperature, and

a plurality of heating elements each proximate to a respective data layer, each heating element in use providing for localized heating of the respective data layer to reduce the coercivity of the data layer so as to facilitate switching of the data layer.

2. (Original) The MRAM of claim 1, wherein:

in use the coercivity of each heated data layer is higher than that of each reference layer.

3. (Original) The MRAM of claim 1, wherein:

in use the coercivity of each heated data layer is lower than that of each reference layer.

4. (Original) The MRAM of claim 1, wherein:

each heating element is a heat-inducing layer.

5. (Original) The MRAM of claim 4, wherein:

each heat-inducing layer is a resistive layer.

6. (Previously Presented) The MRAM of claim 5 wherein:

the resistive layer comprises at least one of the materials Si, Ge, Se, C, SiC, $TaO_2$, WSi, CoSi, FeSi, PtSi, TaN, FeAlN and SiN.

7. (Original) The MRAM of claim 4, wherein:

each heat-inducing layer is a dielectric layer through which in use a tunneling current is directed.

8. (Original) The MRAM of claim 7 wherein:

the dielectric layer comprises at least one of the materials $Al_2O_3$, AlN, $SiO_2$, $Si_3N_4$, BN, MgO and $Ta_2O_5$.

9. (Original) The MRAM of claim 1, wherein:

each heating element is a diode.

10. (Original) The MRAM of claim 9, wherein:

the diode comprises at least one of amorphous silicon and single crystalline silicon.

11. (Original) The MRAM of claim 1, wherein:

each memory device is a tunneling magneto-resistance (TMR) memory device.

12. (Original) A computer system comprising:

a central processing unit,

a main board coupled to the central processing unit and magnetic memory devices coupled to the main board, each magnetic memory device comprising:

an array of magnetic memory cells;

a plurality of word and bit lines connecting columns and rows of the memory cells so that the memory cells are positioned at cross-points of the word and bit lines, each memory cell having a magnetic reference layer and a magnetic data layer, each magnetic reference layer and each magnetic data layer having a magnetization that is switchable between two states under the influence of a magnetic field, each reference layer having at a first temperature a coercivity that is lower than that of each data layer at the first temperature, and

a plurality of heating elements each proximate to a respective data layer, each heating element in use providing for localized heating of the respective data layer to reduce the coercivity of the data layer so as to facilitate switching of the data layer.

13. (Cancelled).

14. (Cancelled).

15. (Cancelled).

16. (Cancelled).